Short Papers

Coplanar Passive Elements on Si Substrate for Frequencies up to 110 GHz

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Abstract—This paper provides both modeling and design information on coplanar passive elements on silicon substrate. The influence of substrate resistivity on coplanar waveguide (CPW) loss is discussed, and elements of a cell library for coplanar monolithic microwave integrated circuits (MMIC's) on high-resistivity substrate are presented. The elements include discontinuities, junctions, and spiral inductors. The models are based on field–theoretical simulations and verified by S-parameter measurements up to 110 GHz.

Index Terms—Branchline coupler, coplanar element library, coplanar elements, silicon substrate, spiral inductor, T-junction.

I. Introduction

Until a few years ago, gallium–arsenide was the only substrate available for integrated designs in the microwave frequency range. Meanwhile, silicon gained a lot of ground in this field. Key advantages of Si-based monolithic microwave integrated circuits (MMIC's) are low wafer costs and compatibility with low-cost and mature processing technology, but beyond 10 GHz, Si is still not competitive with the GaAs counterpart, which is true for power and low-noise applications at lower frequencies as well. Mainly two drawbacks adversely affect Si high-frequency performance: the frequency limits of the active elements, i.e., the transistors, and the poor insulation properties of the common Si substrates which lead to excessive losses of the passive elements. The first-mentioned limits can be overcome by using SiGe heterojunction bipolar transistors (HBT's). The substrate issue can be resolved in two ways: one possibility is to use high-resistivity Si substrates [3], but this wafer material is more expensive than the standard substrates and not fully compatible with common Si processing. An alternative is the use of polyimide line structures on top of the substrate [1], [2].

Thus, the choice of substrate and the characteristics of the passive elements are key problems in the future development of Si MMIC's. Recently, a lot of work has been done in this area [4], [5], but most of the results published refer to single elements such as transmission lines or spiral inductors, and do not bridge the gap to a comprehensive circuit–element library for frequencies beyond 10 GHz. This is the motivation for this paper. The objective is to provide quantitative information on the influence of substrate resistivity and to present design data for MMIC elements up to millimeter-wave frequencies. The considerations focus on the coplanar case.

This paper is organized as follows. In Section II, the influence of substrate resistivity on coplanar waveguide (CPW) performance is
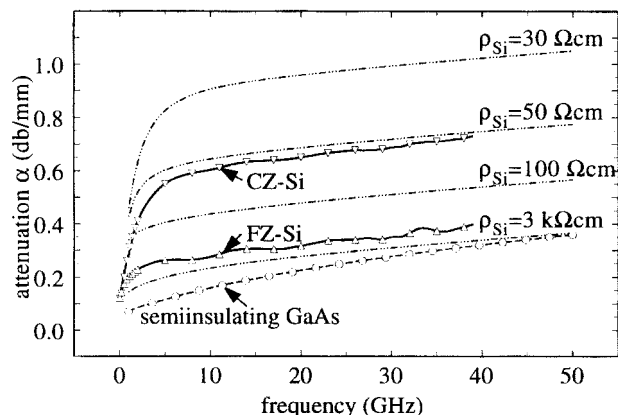
Fig. 1. Attenuation of a coplanar transmission line on Si substrate against frequency. Comparison of simulation data for substrate resistivity values $\rho = 30, \cdots, 3000\ \Omega \cdot \text{cm}$ with measured data on low-resistivity CZ wafer ($\rho \approx 50\ \Omega \cdot \text{cm}$) and high-resistivity FZ-grown material, respectively. The CPW has a 20-μm-wide center conductor, 15-μm slot width, and a 1-μm-thick Al metallization on a 1.2-μm-thick SiO_2 passivation layer. As a reference, the data of the corresponding GaAs line (3-μm-thick Au metallization, no passivation layer) is included.

discussed. The following sections describe modeling of passive coplanar elements on high-resistivity silicon substrate (Section III) and their application in MMIC circuit design up to 77 GHz (Section IV). All technological data for active and passive elements refer to the Daimler-Benz SiGe technology.

II. Influence of Substrate Resistivity

The common Si substrate is low-resistivity material with ρ in the order of $1, \cdots, 100\ \Omega \cdot \text{cm}$. The low resistivity causes considerable losses in the substrate, which increase line attenuation and deteriorate the quality factors of spiral inductors. For typical MMIC geometries, nonideal conductors contribute to the loss as well. Hence, when assessing the influence of substrate resistivity, one has to take into account both loss phenomena. Fig. 1 presents the corresponding data comparing simulation results obtained by means of a mode-matching method [6] with measurements. The cross section is that of a typical MMIC CPW (50-μm ground-to-ground spacing) with 1-μm-thick Al metallization and a SiO_2 layer on top of the Si substrate. This is a common layer structure in Si processes. Additionally, the data for the same line on GaAs is included. In contrast to the Si case, we assume 3-μm-thick Au metallization for the GaAs line, the common metallization scheme for GaAs MMIC's. Since the substrate losses in GaAs are negligible, this curve serves as a reference for the lower loss limit determined by nonideal metallizations.

The results in Fig. 1 point out the following two aspects.

- For the common *low-resistivity (CZ) Si* material, substrate loss is a critical issue. A 50 $\Omega \cdot \text{cm}$ substrate results in approximately twice the attenuation of the comparable line on GaAs, i.e., the line without substrate losses. It is interesting, however, that increasing substrate resistivity pays off well: for 100 $\Omega \cdot \text{cm}$, for instance, the difference in attenuation between the Si, and the GaAs substrate is reduced by 50%.
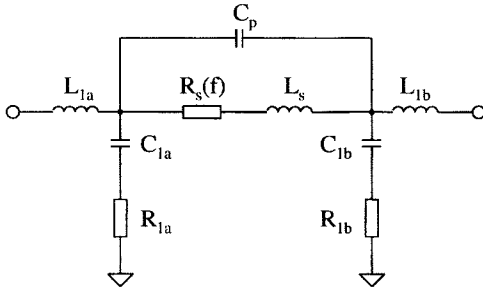
Fig. 2. Equivalent circuit for spiral inductors in coplanar environment (using high-resistivity Si substrate all resistances vanish except for the series resistance $R_{1a} = R_{1b} = 0$).

- For *high-resistivity (FZ) Si* material, substrate loss becomes small compared to metal losses. In this case, using Si or GaAs, the deviations can be neglected. Resistivities in the order of $3 \, k\Omega \cdot cm$ are already sufficient, but one has to be aware of parasitic effects due to surface states in the passivation layer [7], which is required for HBT reliability and dc device isolation. The deviations between the GaAs and Si curves at low frequencies in Fig. 1 originate from the different metal thicknesses.

III. PASSIVE-ELEMENT MODELING

After clarifying the basic effects and eliminating passivation-related parasitics [7], an element library was developed for the Daimler-Benz SiGe MMIC process [3]. The objective was to have available a selection of coplanar passive elements that allows for circuit design of SiGe-HBT MMIC's and Si Schottky-diode-based monolithic mixers for frequencies up to W-band.

The spiral inductors are described by a measurement-extracted equivalent-circuit model, the CPW transmission lines by means of the equivalent-circuit model of [8] which accurately includes loss effects. For the remaining coplanar elements, models were developed applying field-oriented simulation. In a first step, the element is field-theoretically analyzed using the finite-difference method in frequency domain (FDFD) [9]. If necessary, the structure (air–bridge shape, etc.) was modified to optimize microwave characteristics. Then, in a second step, a simplified equivalent-circuit model consisting of lumped inductances, capacitances, and CPW line sections was extracted from the simulation data and verified by measurements. This procedure maintains understanding of the device physics and avoids model uncertainties due to the inevitable scattering of the measured data. The resulting element library can be easily implemented in the common network-oriented computer-aided design (CAD) environment. Only the CPW model [8] has to be included as a special ("user-defined") item.

A complete description of the element library would exceed the scope of this paper. Instead, two examples will be treated in the following, the spiral inductor and the CPW T-junction. The spiral was included because it represents a key element in microwave and RF circuit design and its quality factor is an important figure of merit when comparing Si and GaAs processes. The T-junction serves as an example to illustrate the properties of the CPW element library.

A. Spiral Inductor

Fig. 2 shows the equivalent-circuit model used, the elements of which are extracted from S-parameter measurements. During process development, the effects of passivation on spiral inductor performance were studied. Accordingly, the common spiral equivalent circuit had to be extended by introducing shunt resistances R_{1a} and R_{1b} (see Fig. 2). These elements take into account the conductive
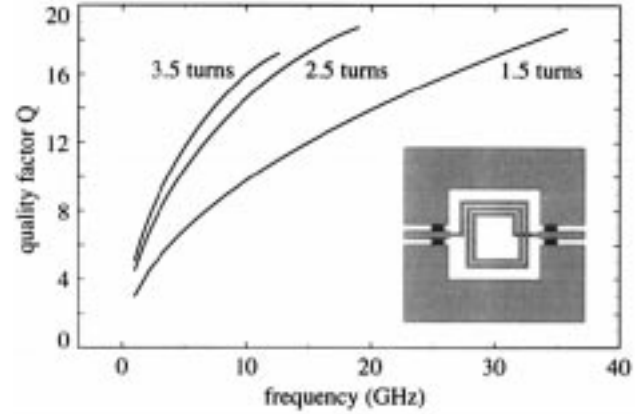

Fig. 3. Quality factor Q against frequency for spiral inductors on high-resistivity Si substrate (for layout see inset, the dimensions are: strip width: 8 μm, spacing between turns: 7 μm, inner diameter: 94 μm, spacing between outer turn and ground: 30 μm).

losses in the substrate caused either by a passivation-induced surface conductivity [7] or by a bulk conductivity. Therefore, the extended circuit applies to the case of low-resistivity Si substrates as well. In the case of high-resistivity substrates processed properly, substrate loss becomes insignificant and the model in Fig. 2 reduces to the common circuit with only one resistance $R_s(f)$.

The quality factor Q of the spiral inductors for a given frequency was determined from the behavior of a resonance circuit formed by the spiral inductor and an ideal shunt capacitance C. The C values were chosen according to the resonance frequency. In Fig. 3, the measurement-extracted Q values of spirals with different numbers of turns on a high-resistivity wafer are plotted (the curves are limited to the resonance frequency of the respective spiral).

We obtain Q values in the range 15, $\cdots$, 20, which are comparable to the GaAs case. This demonstrates that Q is limited by metallization loss, and substrate resistivity does not deteriorate spiral performance any more.

B. CPW T-Junction

Fig. 4 provides details of the structure and the simplified equivalent-circuit model developed. The relatively small values of the circuit elements indicate that the parasitics due to the air–bridge sections and the junction area itself are small, even at millimeter-wave frequencies. This is an important advantage of the coplanar approach with miniaturized CPW geometries, which greatly simplifies modeling compared with the corresponding microstrip case. Loss effects due to the Si substrate can be neglected since they are negligible compared to conductor loss of the homogeneous transmission-line sections. Consequently, an equivalent-circuit topology identical to the GaAs case is chosen. Special attention has to be paid to the passivation layer, which, in our case, is removed in the CPW slots. This geometry reduces effective permittivity and has to be described in detail, e.g., using electromagnetic (EM) simulation tools. Due to its simple structure, the resulting equivalent-circuit model lends itself to implementation in the usual CAD software packages. The model is verified by measurements of a test structure (see Fig. 5).

C. Branchline Coupler

A branchline coupler with a center frequency of 76.5 GHz was used to check accuracy of the models against measurements. This coupler is part of a 77-GHz mixer [10] with the RF frequency at 76.5
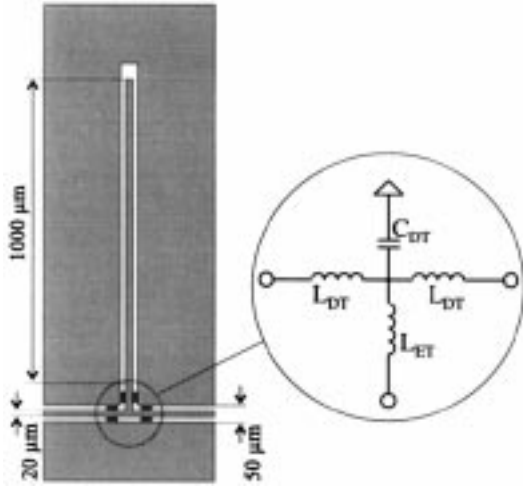
Fig. 4. Geometry of the CPW T-junction embedded in a test structure and the corresponding model. All three branches are 50-Ω CPW lines with 50-μm ground-to-ground spacing (20-μm center conductor, 15-μm slot width) on high-ρ Si substrate with 0.2-μm SiN layer beneath the metallizations. The reference planes are moved 75 μm outwards from the center, the air–bridge sections are 50 μm long. The elements are $C_{DT} = 28$fF, $L_{DT} = 25$pH, and $L_{ET} = 17$pH.
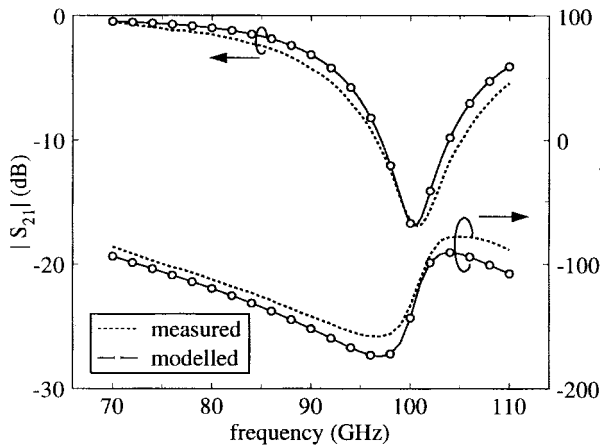

Fig. 5. Comparison of measured and simulated data of the transmission coefficient S_{21} for the T-junction test structure in Fig. 4 for frequencies between 75–110 GHz.

GHz and LO frequency at 75.5 GHz. As explained in Section III-B, T-junction models for different characteristic impedances at the ports were developed. Simulation of the branchline structure in Fig. 6, for instance, requires two different models for a 50–30–50-Ω junction.

Since with the common two-port S parameter measurement equipment it is not possible to terminate unmeasured ports by a frequency-independent matched load, two ports of the coupler are left as open stubs, as depicted in Fig. 6. In this way, one circumvents the problem of matching the unmeasured ports.

Fig. 7 shows transmission magnitude and phase between the ports denoted as "in" and "out" (see Fig. 6). Both $|S_{21}|$ and $\angle S_{21}$ show good agreement up to 110 GHz. The remaining deviations can be attributed to calibration errors and process tolerances. A particular sensitive parameter in this regard is the actual depth of the etching process that removes the SiN between the CPW conductors.

IV. CIRCUIT APPLICATION

Using the passive models of Section III in conjunction with a newly developed Si/SiGe/Si-HBT model [11], [12], we designed
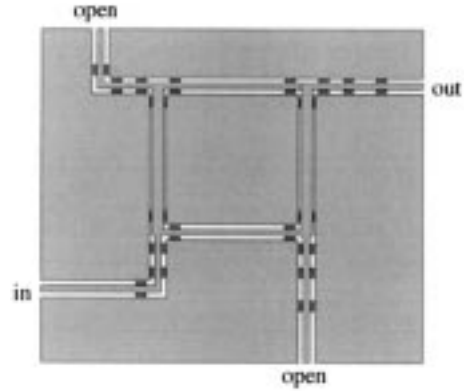

Fig. 6. Layout of the coplanar branchline coupler for a center frequency of 76.5 GHz. The dimensions of the coupler without the feeding at the four ports are 450×450 μm^2. Ground-to-ground spacing of all CPW's is constant (50 μm), for the 35-Ω sections the center-strip width is 35 μm, for the 50-Ω parts it is 20 μm.
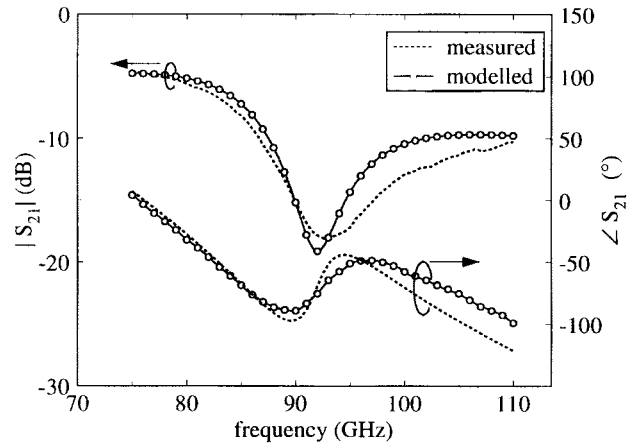

Fig. 7. Measured and modeled transmission coefficient S_{21} of the branch-line test structure in Fig. 6 in the frequency range between 75–110 GHz (transmission between "in" and "out," unmeasured ports left as open stubs).

monolithically integrated LC oscillators at 25- [3] and 38-GHz [13], [14], amplifiers at 25 GHz [15], and Si Schottky diode mixers at 77 GHz [10]. For fabrication, the Daimler-Benz SiGe process was used. The nominal values for all circuits were met with exceptional accuracy. For example, 60% of the measured 38.25-GHz oscillators show a relative deviation from the nominal frequency below 0.1%. This proves usefulness and accuracy of our models.

V. CONCLUSIONS

The microwave performance of Si-based monolithic circuits is basically limited by losses due to substrate resistivity. This restriction can be circumvented only when polyimide or benzocyclobuthene (BCB) thin-film approaches [1], [2] are applied. However, because the MMIC-typical miniaturized line geometries exhibit high conductor loss, substrate loss effects has to be considered in comparison to metallization loss, and their influence differs with the characteristic dimensions of the line one is referring to. Given a typical MMIC CPW with 50-μm ground-to-ground spacing, the following conclusions can be drawn.

- Low-resistivity Si substrates of 50 $\Omega \cdot$cm double the attenuation compared to the GaAs case, which is limited by metallization loss. For resistivity values of 100 $\Omega \cdot$cm, the difference decreases already to 50%. Depending on circuit specifications, therefore,

low-resistivity substrates with $\rho \approx 50 \; \Omega \cdot$ cm and higher may be used in the microwave and low millimeter-wave frequency range.

- High-resistivity (FZ) material is more expensive than the low-ρ counterpart and it requires modifications of the standard Si process steps. On the other hand, one yields a substrate material with low-loss high-frequency features comparable to GaAs. Our results demonstrate that high-resistivity silicon is a substrate suitable for microwave and millimeter-wave applications up to W-band. A coplanar element library was developed based on field-oriented simulation. After implementation in commercial CAD software, the library was successfully employed with MMIC design. In conjunction with SiGe HBT's, a technology exists which meets the requirements for low-cost microwave and millimeter-wave mass products.

ACKNOWLEDGMENT

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Investigation of Microstrip and Coplanar Transmission Lines on Lossy Silicon Substrates Without Backside Metallization

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Abstract—Silicon circuits, now penetrating well into the microwave frequency range, use lossy silicon substrates. Consequently, the microwave performance of transmission lines on this substrate becomes increasingly important and has been investigated here up to 20 GHz. It is shown that transmission lines on 20-$\Omega \cdot$ cm substrates have no need for backside metallization and backside via holes. Two models for different line types are derived from measurements and verified against them. A coplanar waveguide (CPW) with an overall width of less than 30 μm was fabricated with an attenuation of 0.5 dB/mm at 20 GHz, which is acceptable for monolithic microwave integrated circuit (MMIC) design.

Index Terms— Coplanar waveguides, microstrip, MMIC's, silicon, transmission lines.

I. INTRODUCTION

Traditionally, silicon technology uses a medium conducting substrate to balance between isolation characteristics and substrate depletion capacitance [1]. The substrate must be connected to the lowest potential, mostly ground, to put the substrate diodes of the active components in blocking direction. The conductivity of the Si substrate and the need of an oxide on top of the substrate are the major differences to conventional microwave substrates.

Traditional monolithic microwave integrated circuit (MMIC) design on GaAs uses two different line types: microstrip lines (MSL's) with a need for backside metallization and via holes, and coplanar waveguides (CPW's) with problems to suppress odd modes and substrate waves. MSL's on standard Si substrates are very lossy, and the backside metallization is shielded by the substrate for lower frequencies. CPW's are strongly influenced by the substrate, even if the oxide is very thick, because of the need to connect the substrate to ground when active components shall be isolated.

Most of the past work on Si substrate is based on a 1971 paper by Hasegawa *et al.* [2]. The authors distinguish between three types